[0015] **FIG. 2A** illustrates a cross section of another conventional MOS device **200**, which is proposed to solve the misalignment problem shown in **FIG. 1B**. A method to successfully form at least one conductive plug adjacent to at least one poly-silicon gate conductor will be discussed in detail below. STIs **204** first define an active area. A gate dielectric layer **206** is deposited on a semiconductor substrate **202**, and covered by a poly-silicon gate conductor **208**. A low doped drain **210** is formed on the substrate **202**. The upper portion of the poly-silicon gate conductor **208** is alloyed with a metal to form a metal silicide layer **212**. A cap layer **214**, such as an oxide layer, is deposited on top of the metal silicide layer **212**. The gate structure, composed of the poly-silicon gate conductor **208**, the metal silicide layer **212** and the cap layer **214**, is covered on their sidewalls by sidewall spacers **216**. Plus-doped source/drain regions **218** are formed. A salicide source/drain contact **220** is also formed. An inter-level dielectric layer **222** is deposited over the gate structure and the source/drain regions **218**. A via is etched in the inter-level dielectric layer **222**, down to the salicide source/drain contact **220**, and filled with a conductive material forming a conductive plug **224**. A metal layer is then deposited and pattern-etched to form a metal interconnect **226**. Electrical connection is made from the metal interconnect **226**, through conductive plug **224**, to the salicide source/drain contact **220**.

[0016] **FIG. 2B** illustrates a cross section of a conventional MOS device **228**, which is the same as the MOS device **200** in **FIG. 2A**, except that two conductive plugs **230** are misaligned. In such case, the cap layer **214** and the spacer **216** may be partially etched off in the process of forming the via for the conductive plug **230**. The degree of etching of the cap layer **214** depends on the nature of the etchant and the particular material or materials in the cap layer **214**. If the cap layer **214** is thick enough, the silicide layer can be protected from connection to the salicide source/drain contact **220** through the conductive plug **230**.

[0017] From the process perspective, because of the cap layer **214**, it is difficult to form the metal silicide layer **212** and the salicide source/drain contact **220** in the same set of process steps. If the metal silicide layer **212** and the salicide source/drain contact **220** were to be formed simultaneously, the spacers **216** must be formed before a blanket metal layer is deposited, in order to avoid an undesired connection formed therebetween. However, in the present case, the spacers **216** must be formed after the formation of the cap layer **214**. Accordingly, the metal silicide layer **212** must be formed before the cap layer **214** and the spacers **216**. This excludes the metal silicide layer **212** and the salicide source/drain contact layer **220** forming simultaneously. The salicide technology requires a series of process steps, such as metal deposition, thermal treatment, and etching. The conventional MOS devices, as shown in **FIGS. 2A and 2B**, necessitate repeating such salicide process steps twice. This significantly increases the fabrication overhead. While the cap layer **214** avoids the misalignment problem, it complicates the fabrication process and increases costs.

[0018] **FIG. 3A** illustrates a cross section of a MOS device **300** constructed on a semiconductor substrate **302**, such as Si, SiGe, epi-Si and Ge, in accordance with the first embodiment of the present invention. STIs **304** define an active area, on which the MOS device **300** is formed. A gate dielectric layer **306** is formed on the substrate **302**, and covered by a metal gate conductor **308**. The metal gate conductor **308** has a thickness between 100 and 3,000 Angstroms. The material of the metal gate conductor **308** can be a refractory metal, nitrided metal, tungsten (W), aluminum (Al), aluminum/copper (AlCu), copper (Cu), copper content, metal silicide, titanium (Ti), titanium silicide ($TiSi_2$), cobalt (Co), cobalt silicide ($CoSi_2$), nickel (Ni), nickel silicide (NiSi), titanium nitride (TiN), titanium/tungsten (TiW), tantalum nitride (TaN), or a combination thereof. The gate dielectric layer **306** can be oxide, silicon oxide, silicon oxynitride (SiON), silicon nitride (Si_3N_4), tantalum oxide (Ta_2O_5), alumina (Al), hafnium oxide (HfO), plasma-enhanced chemical vapor deposition (PECVD) oxide, tetraethylorthosilicate (TEOS), nitrogen content oxide, nitrided oxide, hafnium content oxide, tantalum content oxide, aluminum content oxide, high K (K>5) material, or a combination thereof.

[0019] A low doped drain **310** is diffused. A cap layer **312**, having a thickness between 50 and 3,000 Angstroms, is formed atop the metal gate conductor **308**. Appropriate materials of the cap layer **312** include oxide, silicon oxynitride, silicon nitride, tantalum oxide, alumina, hafnium oxide, plasma enhanced chemical vapor deposition (PECVD) oxide, tetraethylorthosilicate (TEOS). Nitrogen content oxide, nitrided oxide, hafnium content oxide, tantalum content oxide, aluminum content oxide, high K (K>5) material, or a combination of two or more. In this embodiment, the cap layer **312** can be a single layer or multiple layers, such as, an oxide layer or a layer of oxide covered by a layer of silicon nitride, wherein the oxide layer has a thickness between 50 and 3,000 Angstroms, and the silicon nitride layer has a thickness between 50 and 2,000 Angstroms.

[0020] The gate stack, composed of the metal gate conductor **308** and the cap layer **312**, is covered on their sidewalls by sidewall spacers **314**. Appropriate materials of the side wall spacers **314** include oxide, silicon oxynitride, silicon nitride, low pressure TEOS (LPTEOS), high temperature oxide (HTO), furnace oxide, plasma-enhanced chemical enhanced deposition (PECVD) oxide, low pressure (LP) oxide, low K (K<3.1), hafnium content oxide, tantalum content oxide, aluminum content oxide, high K (K>5) material, oxygen content dielectric, nitrogen content dielectric, or a combination thereof. This dielectric sidewall spacer **314** serves as an isolation dielectric layer between the metal gate conductor **308** and an adjacent self-aligned contact **318** and a conductive plug **322**.

[0021] A plus-doped source/drain regions **316** are formed on the substrate **302**. A salicide source/drain contact **318** is then formed adjacent to the metal gate conductor **208** on the substrate **302**. An inter-level dielectric layer **320**, such as a silicon oxide layer, is deposited over the sour/drain regions **316**, the spacers **314** and the cap layer **312**. A contact via is etched through the inter-level dielectric layer **320**, down to the salicide source/drain contact **318**, and filled with a conductive material, forming a conductive plug **322**. Appropriate conductive materials for the plug **322** include refractory metal, nitrided metal, tungsten, aluminum, aluminum/copper, copper, copper content, silicide, titanium, titanium silicide, cobalt, cobalt silicide, nickel, nickel silicide, titanium nitride, tantalum nitride, or a combination thereof. The conductive plug **322** and the salicide source/drain contact **318**, together, are referred to as a self-aligned contact